LP38856S-1.2 Evaluation Board

National Semiconductor
Application Note 1479
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Introduction

This board is designed to allow the evaluation of the LP38856S-1.2 Voltage Regulator. Each board is assembled and tested in the factory. This evaluation board has the TO-263 5-lead package mounted.

General Description

The LP38856 is a dual-rail LDO linear regulator capable of suppling up to 3A of output current, and incorporates an Enable function

The device has been designed to work with 10 µF input and output ceramic capacitors, and 1µF bias capacitors. Footprints areas for C_{IN} and C_{OUT} will allow for a variety of sizes.

Operation

The input voltage, applied between V_{IN} and GND, should be at least 1.0V greater than V_{OUT}, and no higher than the applied V_{BIAS} voltage.

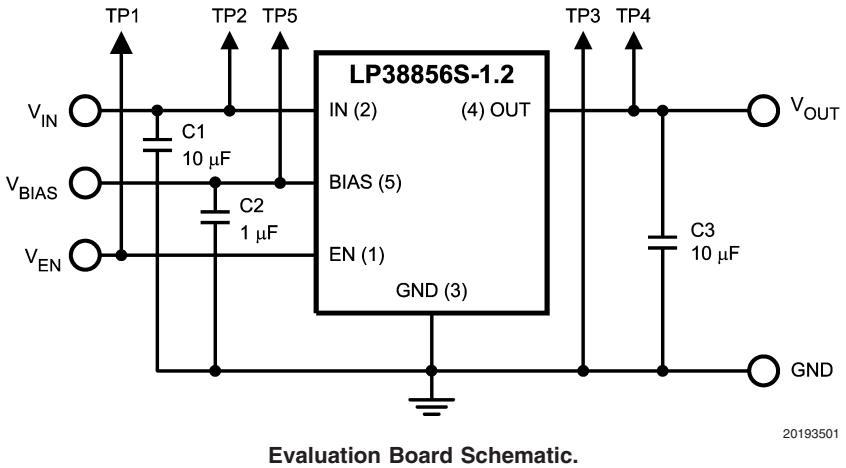
The bias voltage, applied between V_{BIAS} and GND should be above the minimum bias voltage of 3.0V, and no higher than the maximum of 5.5V.

Loads can be connected to V_{OUT} with reference to GND.

V_{OUT} and V_{IN} test points are provided on the board to allow accurate measurements directly on the evaluation board, eliminating any voltage drop on the PCB traces or connecting wires to the load.

ON/OFF control is provided by supplying a logic level signal to the Enable pin. A minimum V_{EN} value of 1.3V is required at this pin to enable the LDO output. The LDO output will be shutdown when the V_{EN} value is 1.0V or less. The V_{EN} threshold incorporates approximately 100mV of hysteresis.

Schematic Diagram



Evaluation Board Schematic.

In applications were the LP38856 is operated continuously the Enable pin can be connected directly to V_{BIAS}, or left open. The Enable pin has a 200 kΩ internal resistor to V_{BIAS}. If the Enable pin is left open, care should be taken to minimize any capacitance on the Enable pin, as any capacitance will introduce an RC delay time on the Enable function.

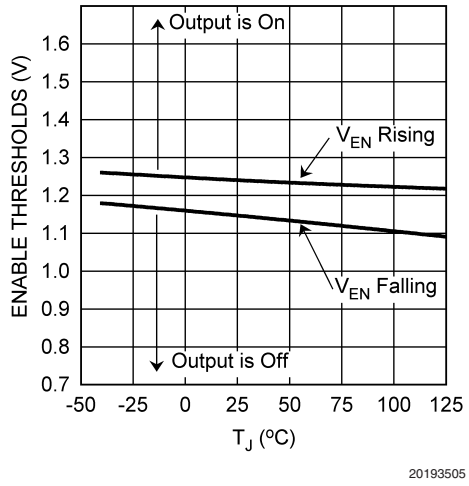


FIGURE 1. Enable Thresholds

Hardware

The schematic and layout of the evaluation board are given below:

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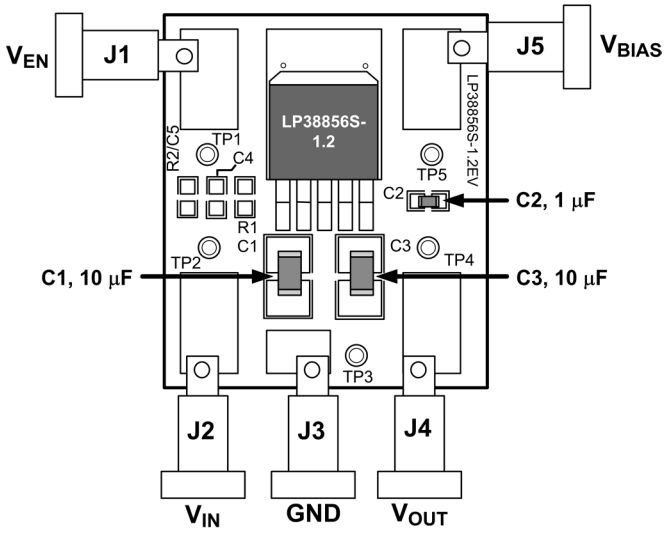
PCB Layout



Evaluation Board Component and Pin Layout

Power Dissipation

The TO-263 package alone has a junction to ambient thermal resistance (θ_{JA}) rating of 60˚C/W. When mounted on the LP38856S evaluation board the θ_{JA} rating is approximately 37˚C/W.

Although there is only approximately 0.28 square inches of copper area immediately under the tab, the top copper surface area is extended to additional copper area on the bottom of the board by five thermal vias.

With the 37˚C/W thermal rating the LP38856S evaluation board will dissipate a maximum of 2.75W with T_A = 25˚C.

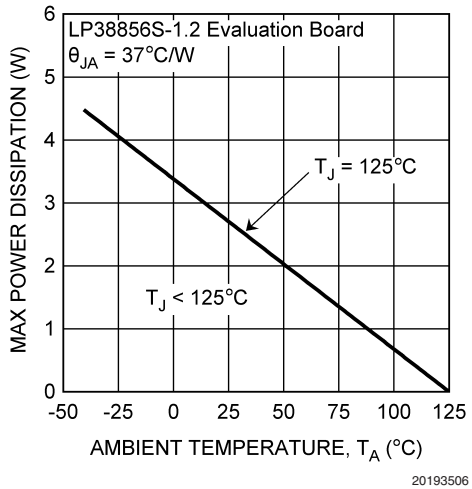


FIGURE 2. Maximum Power Dissipation vs Ambient Temperature

Bill of Materials

ID	Name	Description	Manufacturer	Part Number
U1	U1	LP38856S-1.2 NOPB	National Semiconductor Corporation	LP38856S-1.2 NOPB
C1	C_{IN}	10 µF, 10%, MLCC, 10V, X7R, 1210	AVX	1210ZC106KAT2A
C2	C_{BIAS}	1 µF, 10%, MLCC, 10V, X7R, 0805	AVX	0805ZC105KAT2A
C3	C_{OUT}	10 µF, 10%, MLCC, 10V, X7R, 1210	AVX	1210ZC106KAT2A
C4	—	Not Installed	—	—
C5	—	Not Installed	—	—
J1	V_{EN}	Banana Jack : Insulated Solder Terminal - WHITE	Johnson Components	108-0901-001
J2	V_{IN}	Banana Jack : Insulated Solder Terminal - RED		108-0902-001
J3	GND	Banana Jack : Insulated Solder Terminal - BLACK		108-0903-001
J4	V_{OUT}	Banana Jack : Insulated Solder Terminal - ORANGE		108-0906-001
J5	V_{BIAS}	Banana Jack : Insulated Solder Terminal - BLUE		108-0910-001
R1	—	Not Installed	—	—
R2	—	Not Installed	—	—
TP1	TP_{EN}	Turret Terminal : Mounting Hole Diameter = 0.062”	Keystone	1593–2
TP2	TP_{IN}			
TP3	TP_{GND}			
TP4	TP_{OUT}			
TP5	TP_{BIAS}			

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